Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1(original): A method of forming at least one semi-insulating region in a semiconductor substrate, the method comprising:

forming at least one first mask above the semiconductor substrate, the first mask blocking the semi-insulating region;

forming a second mask on a surface of the semiconductor substrate, the second mask covering the semi-insulating region;

implanting the semi-insulating region with a high energy beam of particles by utilizing the second mask and the first mask as particle hindering masks; and

removing the second mask.

Claim 2(original): The method of claim 1 wherein the semiconductor substrate comprises a silicon substrate, a germanium substrate, a gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride substrate, a silicon carbide substrate, or a silicon on insulator (SOI) substrate.

Claim 3(original): The method of claim 1 wherein a plurality of nonadjacent non-insulating regions are comprised on the surface of the semiconductor substrate.

Claim 4(original): The method of claim 3 wherein a plurality of nonadjacent first patterns are defined in the first mask, each first pattern is used for defining the plurality of nonadjacent non-insulating regions.

Claim 5(withdrawn): The method of claim 4 wherein the first pattern has a plurality of

thicknesses.

Claim 6(original): The method of claim 3 wherein a plurality of nonadjacent second patterns are defined in the second mask, each second mask is used for defining the plurality of nonadjacent non-insulating regions.

Claim 7(withdrawn): The method of claim 6 wherein the second pattern has a plurality of thicknesses.

Claim 8(original): The method of claim 1 wherein to implant the semi-insulating region with the high energy beam of particles is to damage the structure of the semiconductor substrate to a specific depth in the semi-insulating region so as to increase the resistivity of the semiconductor substrate in the semi-insulating region.

Claim 9(original): The method of claim 1 wherein at least one first isolation layer is comprised on the surface of the semiconductor substrate.

Claim 10(original): The method of claim 9 wherein at least one active device and at least one passive device are comprised between the surface of the semiconductor substrate and the first isolation layer.

Claim 11(original): The method of claim 10 wherein the active device comprises a metal-oxide-semiconductor transistor (MOS transistor), a bipolar junction transistor (BJT), or a power amplifier, and the passive device comprises an antenna, a high quality factor inductor (high Q inductor), a power divider, a filter, a resonator, a transmission line, or a coupler.

Claim 12(original): The method of claim 10 wherein the second mask is a composite

layer and the composite layer is a stacked structure of a patterned photoresist layer and a second isolation layer from top to bottom.

Claim 13(original): The method of claim 12 wherein the second isolation layer comprises a silicon oxide layer (SiO_x layer, $0<x\leqq 2.0$), a silicon nitride layer (SiN_y layer, $0<y\leqq 1.33$), or a silicon oxynitride layer (SiO_xN_y layer, $0<x\leqq 2.0$, $0<y\leqq 1.33$) formed by a low temperature process.

Claim 14(original): The method of claim 13 wherein a multilevel metallization process is performed before forming the second isolation layer to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

Claim 15(original): The method of claim 13 wherein a lower level metallization process is performed before forming the second isolation layer, an upper level metallization process is performed after removing the second mask to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

Claim 16(original): The method of claim 10 wherein a multilevel metallization process is performed after removing the second mask to electrically connect the active device and the passive device to at least one bonding pad, at least one metal line, or at least one interconnect.

Claim 17(original): The method of claim 10 wherein at least one third isolation layer is comprised between the semiconductor substrate and the device in the semi-insulating region.

Claim 18(original): The method of claim 1 wherein the first mask comprises a patterned dummy wafer or a metal plate formed from a high atomic weight metal material.

Claim 19(original): The method of claim 18 wherein the dummy wafer comprises a silicon substrate, a germanium substrate, a gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride substrate, a silicon carbide substrate, or a silicon on insulator (SOI) substrate.

Claim 20(original): The method of claim 1 wherein the second mask is a patterned photoresist layer.

Claim 21(original): The method of claim 1 wherein the high energy particles comprise protons, hydrogen atoms, deuterons, tritons, alpha (α) particles, molecular nitrogen ions, or molecular oxygen ions.

Claim 22(original): The method of claim 1 wherein to implant the semi-insulating region with the high energy beam of particles is to make the high energy beam of particles penetrate through the semiconductor substrate outside the semi-insulating region so as to prevent the structure of the semiconductor substrate outside the semi-insulating region from being damaged.

Claim 23(original): The method of claim 22 wherein the semiconductor substrate penetrated through by the high energy beam of particles is not insulated.

Claims 24-56(canceled).